Part Number: IGN0110UM100

Integra
TECHNOLOGIES, INC.

Broadband Transistor

IGN0110UM100 is a dual gallium nitride (GaN) high electron mobility transistor (HEMT). This device is designed for Broadband applications operating over the 100MHz – 1GHz instantaneous frequency band. Under CW conditions it supplies a minimum of 100 watts of output power with 12dB gain. Specified operation is with Class AB bias. It is also operable under a wide range of pulse widths and duty factors. It operates with spectral purity into all phases of 3:1 output load VSWR. All devices are 100% screened for large signal RF parameters in a fixed tuned broadband matching circuit / test fixture. The use of external tuners is not allowed during screening.

GaN on Silicon Carbide FET
- High Power Gain
- Excellent Thermal Stability
- Gold Metal

Depletion Mode Device
- Negative Gate Voltage to Bias
- Bias Sequencing Required
- See App Note to Prevent Damage

Gold Metal System
- Complete Gold System
- Gold Bond Wires
- Gold Package Metal
- Maximum Reliability

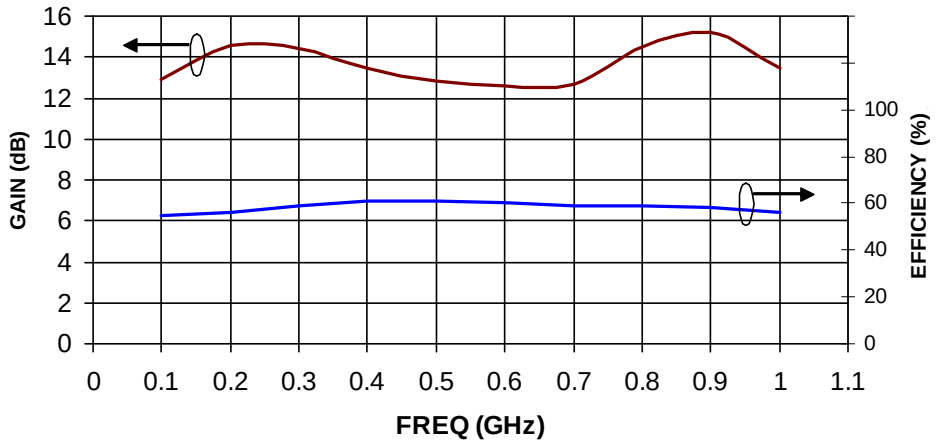
Class AB
- Specified with AB bias

Metal - Ceramic
- Metal Based
- Epoxy Seal

High Power RF Test / Fixture
- Broadband
- Matched to 50 Ω (ohms)
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

B R O A D B A N D R F D A T A

Output Power = 100W CW
Vdd = 28V, Idq = 480mA



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MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	60	V	--
BD	Gate-Source Voltage	V_{GS}	-10	0	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.50	°C/W	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=25±5°C, P_{OUT}=100W
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
100%	Drain Leakage Current	I_{D-OFF}	--	0.6	--	mA	V_{GS} = -8V, V_{DS} = 28V, T_F = 25±5°C, Per Side
100%	Gate Threshold Voltage	V_{GS-TH}	--	-3.5	--	V	V_{DS} = 5V, I_D = 480mA, T_F = 25±5°C, Per Side

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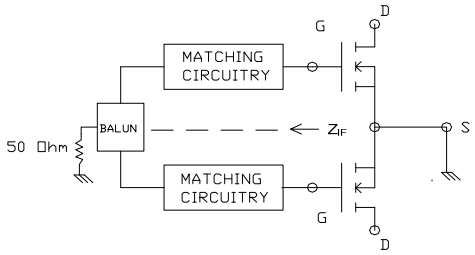
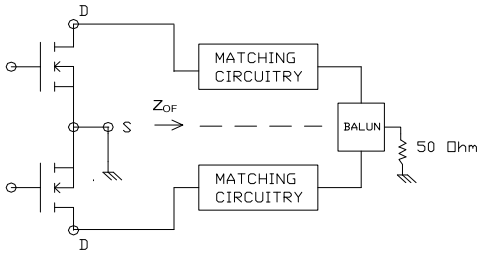
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	RL	-18	-5	dB	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{OUT}=P_{OUT1}, F=F1, F2, F3.
100%	Output Power	P_{IN}	2.5	6.3	W	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{OUT}=P_{OUT1}, F=F1, F2, F3.
100%	Drain Efficiency	N_D	50	75	%	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{OUT}=P_{OUT1}, F=F1, F2, F3.
100%	Power Gain	Gp	12	16	dB	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{OUT}=P_{OUT1}, F=F1, F2, F3.
100%	3:1 Load Mismatch Stability	VSWR-S	S	--	--	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{OUT}=P_{OUT1}, F=F1, F2, F3. Rotate 3:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least –65 dBc.
Note 1	V1 = 28V; I_{DQ1} = 480mA; PW1 = CW; DF1 = CW					
Note 2	Output Power Test Levels: P_{OUT1} = 100W					
Note 3	Test Frequencies: F1 = 0.1 GHz, F2 = 0.6 GHz, F3 = 1.0 GHz.					
Note 4	T_{F1} = 25±5°C = Device flange temperature.					
Note 5	Screen 'BD' = parameter qualified By Design.					

RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (GHz)	Z_{IF} (Ω)	Z_{OF} (Ω)
0.1	10.2 + j 0.6	11.3 – j 2.7
0.3	13.5 – j 1.1	10.8 – j 4.7
0.6	8.1 – j 6.2	7.8 – j 7.2
0.8	6.2 – j 4.8	4.3 – j 9.2
1.0	6.3 – j 12.3	1.3 – j 8.3
Differential Impedance Definition		

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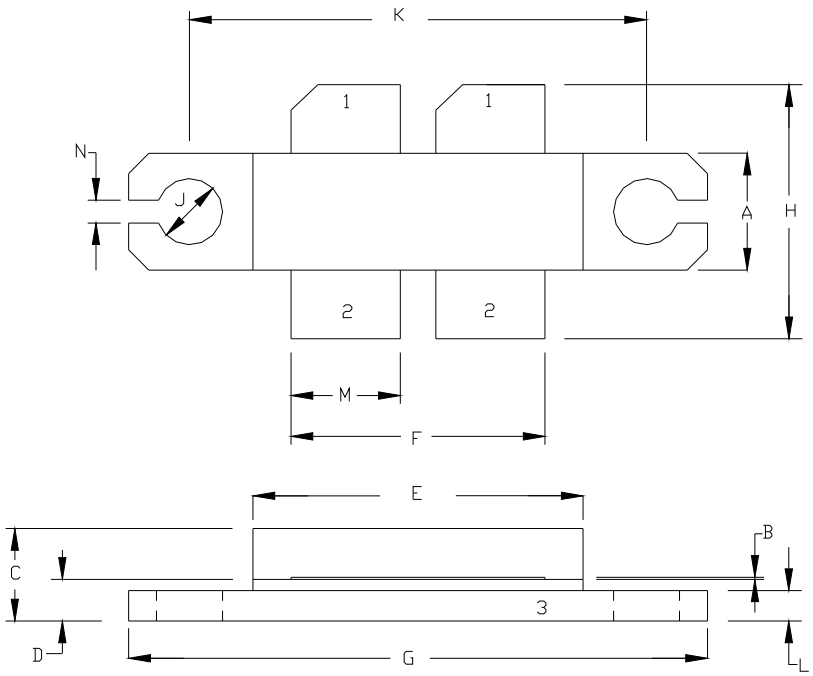
PACKAGE DIMENSIONAL OUTLINE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.225	0.235	5.72	5.97
B	0.003	0.005	0.08	0.13
C	0.177	0.187	4.50	4.75
D	0.077	0.087	1.96	2.21
E	0.645	0.655	16.38	16.64
F	0.495	0.505	12.57	12.83
G	1.135	1.145	28.83	29.08
H	0.490	0.510	12.44	12.95
J	0.128	0.132	3.25	3.35
K	0.895	0.905	22.73	22.99
L	0.055	0.065	1.40	1.65
M	0.210	0.220	5.35	5.60
N	0.040	0.050	1.02	1.27

PIN SCHEDULE	
1	DRAIN
2	GATE
3	SOURCE

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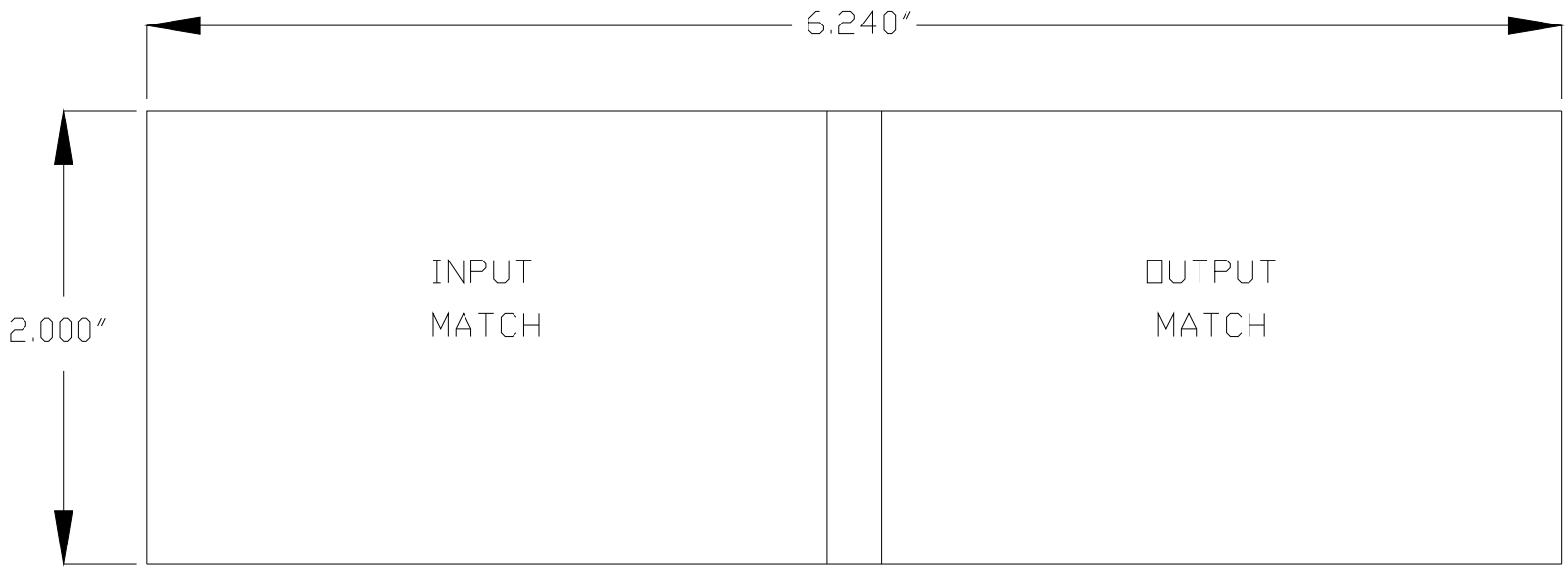
RF TEST FIXTURE



CONTACT FACTORY FOR RF TEST FIXTURE CAD DRAWING WITH CIRCUIT DIMENSIONS AND COMPONENT LIST

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DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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